REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Made technical changes in table I. Editorial changes throughout document.	1990 DEC 5	William K. Heckman

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REV STATUS OF SHEETS	REV	A	A				A	A						A											
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13											

PMIC N/A

STANDARDIZED MILITARY DRAWING

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AMSC N/A

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DRAWING APPROVAL DATE: 20 MARCH 1990

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANCED LOW POWER SCHOTTKY TTL, OCTAL BUS TRANSCEIVERS AND REGISTERS, WITH INVERTING THREE-STATE AND OPEN COLLECTOR OUTPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-89687

SHEET 1

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1738

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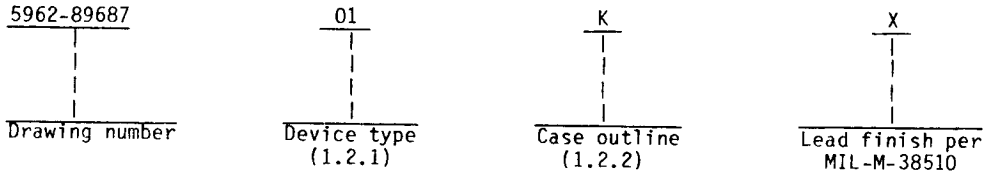
1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ALS653	Octal bus transceivers and registers with inverting three-state and open-collector outputs

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
K	F-6 (24-lead, .640" x .420" x .090"), flat package
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
3	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage:	
All inputs and A I/O ports	-1.2 V dc at -18 mA to +7.0 V dc
B I/O ports	-1.2 V dc at -18 mA to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	484 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C

1/ Maximum power dissipation is defined as V_{CC} x I_{CC}, and must withstand the added P_D due to short-circuit output test; e.g., I_O.

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1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL}):	
T_C = +125°C	0.7 V dc
T_C = -55°C	0.8 V dc
T_C = +25°C	0.8 V dc
Maximum high level output voltage (V_{OH}) A ports	5.5 V dc
Maximum high level output current (I_{OH}) B ports	-12 mA
Maximum low level output current (I_{OL})	+12 mA
Case operating temperature range (T_C)	-55°C to +125°C
Minimum setup time, before CAB or before CBA (t_s) 2/	15.0 ns
Minimum hold time, after CAB or after CBA (t_h) 2/	5.0 ns
Minimum pulse duration (t_w):	
CBA or CAB high	25.0 ns
CBA or CAB low	25.0 ns
Maximum clock frequency (f_{clock}):	
A output	12.5 MHz
B output	25 MHz

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standarized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

2/ Transition of clock from high to low.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Test circuits and switching waveforms. The test circuits and switching waveforms shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ 1/ unless otherwise specified			Group A subgroups	Limits Min	Limits Max	Unit
High level output voltage B ports	V_{OH}	V_{CC} = 4.5 V V_{IH} = 2.0 V 2/	V_{IL} = 0.8	I_{OH} = -0.4 mA I_{OH} = -3.0 mA I_{OH} = -12 mA	1,3	2.5 2.4 2.0		V
			V_{IL} = 0.7	I_{OH} = -0.4 mA I_{OH} = -3.0 mA I_{OH} = -12 mA	2	2.5 2.4 2.0		
Low level output voltage	V_{OL}	V_{CC} = 4.5 V V_{IH} = 2.0 V I_{OL} = 12 mA 2/	V_{IL} = 0.8 V		1,3		0.4	V
			V_{IL} = 0.7 V		2		0.4	
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 mA			1,2,3		-1.2	V
High level input current	I_{IH1}	V_{CC} = 5.5 V 3/	V_{IN} = 7.0 V Control inputs		1,2,3		0.1	mA
			V_{IN} = 5.5 V A or B ports				0.1	
	I_{IH2}		V_{IN} = 2.7 V Control inputs				20	µA
			V_{IN} = 2.7 V A or B ports				20	
Low level input current	I_{IL}	V_{CC} = 5.5 V 3/	V_{IN} = 0.4 V Control inputs		1,2,3		-0.2	mA
			V_{IN} = 0.4 V A or B ports				-0.2	
Low level output current	I_{OH}	V_{CC} = 4.5 V V_{OH} = 5.5 V	A port		1,2,3		0.1	mA
Output current	I_O	V_{CC} = 5.5 V V_{OUT} = 2.25 V 4/	B ports		1,2,3	-30	-112	mA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Supply current	I_{CCH}	V_{CC} = 5.5 V	Outputs high	1,2,3		76	mA
	I_{CCL}		Outputs low			88	
	I_{CCZ}		Outputs disabled			88	
Functional tests		See 4.3.1c 5/		7,8			
Maximum frequency	f_{max}	V_{CC} = 4.5 to 5.5 V dc C_L = 50 pF $R_1 = R_2$ = 500Ω See figure 3 6/	A output	9,10,11	12.5		MHz
			B output		25		
Propagation delay time, CBA to A	t_{PLH1}			9,10,11	16	71	ns
	t_{PHL1}				6	24	
Propagation delay time, CAB to B	t_{PLH2}			9,10,11	10	35	ns
	t_{PHL2}				5	20	
Propagation delay time, A to B	t_{PLH3}			9,10,11	5	20	ns
	t_{PHL3}				1.5	18	
Propagation delay time, B to A	t_{PLH4}			9,10,11	8	63	ns
	t_{PHL4}				2	18	
Propagation delay time, SBA to A (with B low) 7/	t_{PLH5}			9,10,11	12	68	ns
	t_{PHL5}				5	27	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
Propagation delay time, SBA to A (with B high) 7/	t_{PLH6}	V_{CC} = 4.5 to 5.5 V dc C_L = 50 pF $R_1 = R_2 = 500\Omega$ See figure 3 6/	9,10,11	19	68	ns
	t_{PHL6}			5	27	
Propagation delay time, SAB to B (with A low) 7/	t_{PLH7}		9,10,11	12	40	ns
	t_{PHL7}			6	25	
Propagation delay time, SAB to B (with A high) 7/	t_{PLH8}		9,10,11	8	30	ns
	t_{PHL8}			6	25	
Propagation delay time, $\overline{GBA}$ to A	t_{PLH9}		9,10,11	6	35	ns
	t_{PHL9}			6	27	
Output enable time, GAB to B	t_{PZH1}		9,10,11	7	25	ns
	t_{PZL1}			6	25	
Output disable time, GAB to B	t_{PHZ1}		9,10,11	1	16	ns
	t_{PLZ1}			2	21	

1/ Unused inputs that do not directly control the pin under test must be put at $\ge$ 2.5 V or $\le$ 0.4 V. No unused inputs shall exceed 5.5 V or go less than 0.0 V. No inputs shall be floated.
2/ All outputs must be tested. In the case where only one input at V_{IL} maximum or V_{IH} minimum produces the proper state, the test must be performed with each input being selected as the V_{IL} maximum or V_{IH} minimum input.
3/ For I/O ports, the parameters I_{IH2} and I_{IL} include the off-state output current.
4/ The output conditions have been chosen to produce a current that closely approximates one-half of the true short circuit output current, I_{OS}. Not more than one output will be tested at one time and duration of the test condition shall not exceed 1 second.
5/ Functional tests shall be conducted at input test conditions of GND $\le V_{IL} \le V_{OL}$ and $V_{OH} \le V_{IH} \le V_{CC}$.
6/ Propagation delay limits are based on single output switching. Unused inputs = 3.5 V or $\le$ 0.3 V.
7/ These input parameters are measured with the internal output state of the storage register opposite to that of the bus input.

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Device type	01	
Case outlines	K and L	3
Terminal number	Terminal symbol	
1	CAB	NC
2	SAB	CAB
3	GAB	SAB
4	A1	GAB
5	A2	A1
6	A3	A2
7	A4	A3
8	A5	NC
9	A6	A4
10	A7	A5
11	A8	A6
12	GND	A7
13	B8	A8
14	B7	GND
15	B6	NC
16	B5	B8
17	B4	B7
18	B3	B6
19	B2	B5
20	B1	B4
21	$\overline{GBA}$	B3
22	SBA	NC
23	CBA	B2
24	V_{CC}	B1
25	---	$\overline{GBA}$
26	---	SBA
27	---	CBA
28	---	V_{CC}

NC = No connection

FIGURE 1. Terminal connections.

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Inputs						Data I/O		Operation or function
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A1 thru A8	B1 thru B8	
L	H	H/L	H/L	X	X	Input	Input	Isolation
L	H	↓	↓	X	X	Input	Input	Store A and B data
X	H	↓	H/L	X	X	Input	Unspecified (see note 1)	Store A, hold B
H	H	↓	↓	X (see note 2)	X	Input	Output	Store A in both registers
L	X	H/L	↓	X	X	Unspecified (see note 1)	Input	Hold A, store B
L	L	↓	↓	X	X (see note 2)	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time $\overline{B}$ data to A bus
L	L	X	H/L	X	H	Output	Input	Stored $\overline{B}$ data to A bus
H	H	X	X	L	X	Input	Output	Real-time $\overline{A}$ data to B bus
H	H	H/L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus
H	L	H/L	H/L	H	H	Output	Output	Stored $\overline{A}$ data to B bus and stored $\overline{B}$ data to A bus

H = High level voltage
L = Low level voltage
H/L = High or low level voltage
X = Irrelevant
↓ = Transition of clock from high to low

NOTES:
1. The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enable, i.e., data at the bus pins will be stored on every low to high transition of the clock inputs.
2. Select control = L: Clocks can occur simultaneously.
   Select control = H: Clocks must be staggered in order to load both registers.

FIGURE 2. Truth table.

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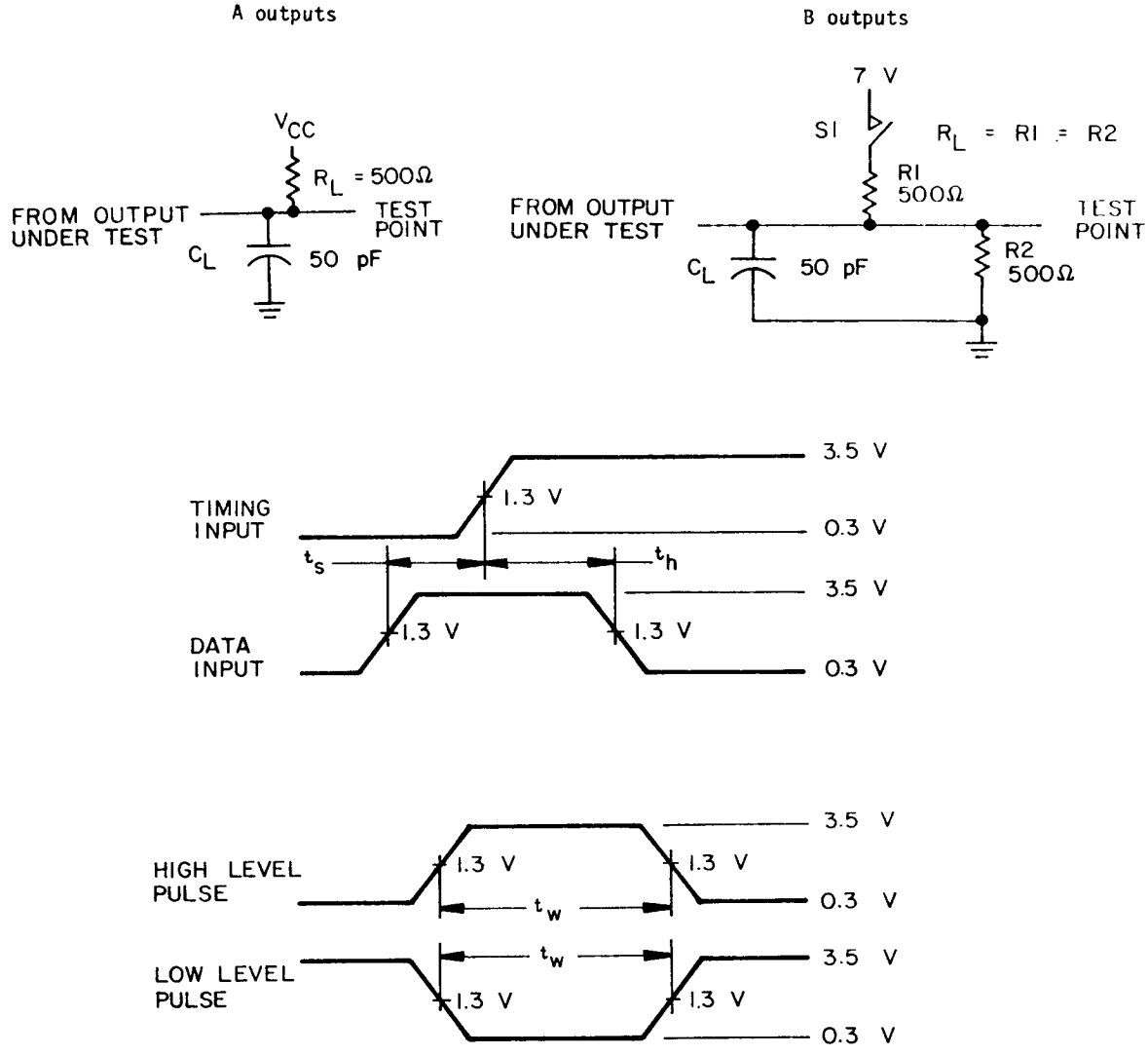

FIGURE 3. Test circuits and switching waveforms.

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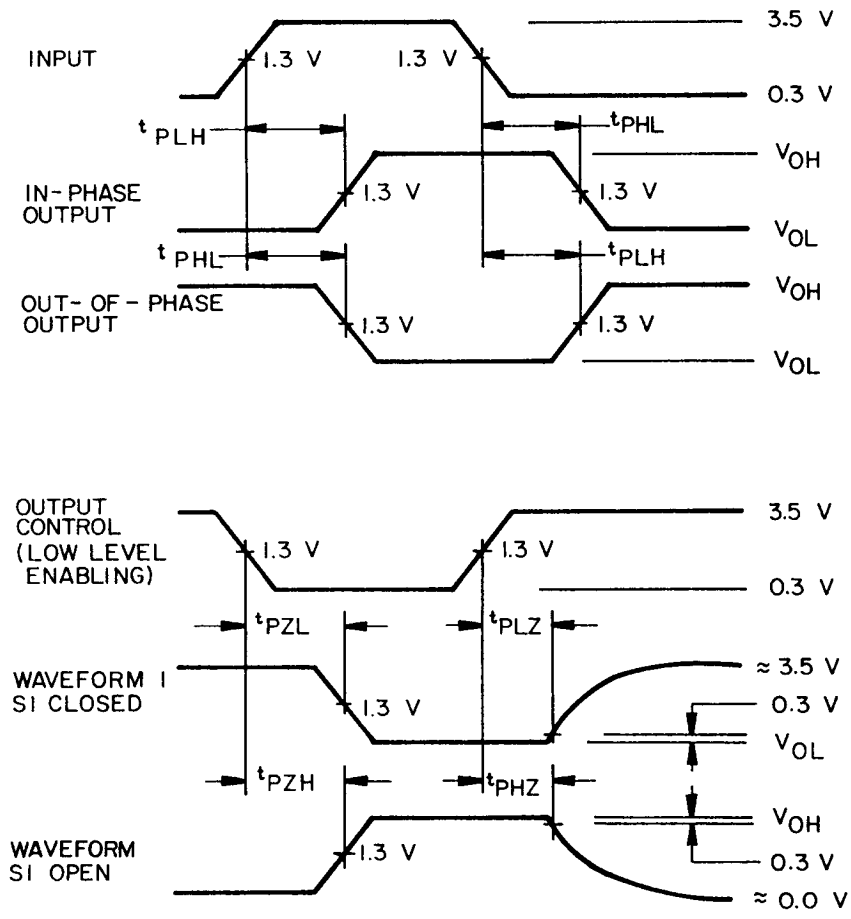

NOTES:
1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
3. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. When measuring propagation delay times of three-state outputs, switch S1 is open.
5. The outputs are measured one at a time with one input transition per measurement.
6. All input pulses have the following characteristics: PRR $\leq$ 10 MHz, duty cycle = 50 percent, $t_r = t_f$ = 3 ns ±1 ns.
7. Also requires load circuit for open-collector outputs.

FIGURE 3. Test circuits and switching waveforms - Continued.

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 tests shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.

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